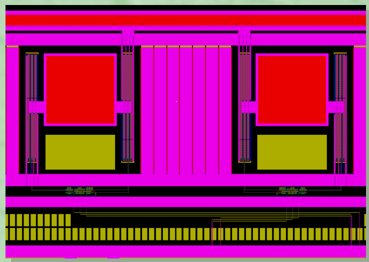


Green Arrays™ F18A

I/O and Peripherals

FEATURES

- Software Defined I/O
- High impedance (<3pF, >200MΩ) inputs
- Low power outputs
- ESD protection ≈1KV HBM
- Single **io** control and status register
- General purpose digital I/O pins
- Pin wakeup
- Analog Input and Output
- High speed SERDES
- 18-bit Parallel Bus

SIGNATURE F18 PROPERTIES

- Input pins can be less invasive than most scope probes.
- Encourages efficient system design
- Flexibility and software control of I/O promote simple, innovative designs

APPLICATIONS

- Simple digital input and output points
- Simple communications PHY such as
  - Asynchronous RS232 framing
  - Synchronous, clock and data
  - High speed async >10 Mbit/sec
  - High speed sync ≈450 Mbit/sec
  - Low speed USB PHY
  - 10baseT PHY
- Complex interfaces such as
  - SRAM/SDRAM control
  - SPI bus master or slave
- Real world interfaces such as
  - Temperature sensors
  - LEDs and photodetectors
  - Shaft encoders
  - Stepper or DC motors
  - Low band software defined radio
  - Human neurons
- Novel systems approaches, such as
  - Software operated resonant devices
  - Software TDR
- A wealth of applications not yet imagined or explored
- Featured in GreenArrays G144A12

OVERVIEW

The F18A computer's I/O repertoire consists of four classes of pins with peripheral circuitry: General Purpose programmable digital I/O, Analog I/O, 18-bit parallel buses, and a high speed serializer/deserializer (SERDES). Chips may be created with any practical combination of these classes connected to selected edge nodes; the actual functions of the pins are defined by software running in the nodes.

I/O PINS IN GENERAL: When used for input, our pins are designed to represent high-impedance loads with little capacitance. For output, we design for driving small, capacitive loads, to minimize I/O energy consumption. Some pins are capable of higher power modes of operation. Each pin has ESD protection diodes which begin conducting (.1µA) when the voltage at a pin reaches ≈Vdd+180mV or ≈Vss-100mV. ESD testing of prototype chips indicates Human Body Model protection on the order of 1KV.

THE IO REGISTER: An 18-bit control and status register, named **io** and diagrammed below, is each F18A's interface with its I/O circuitry (if any) and comm port handshake lines. In the "READ" line of the table below, the green background indicates signals that, if they exist, come from other nodes or the world outside. If not, they are treated like

BIT	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reset	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
WRITE	pin 17	ctl					WD						pin 5	ctl	pin 3	ctl	pin 1	ctl
Alt write	SR			vco	ctl	DB				9 bit D/A val (155 xor)								
READ	pin 17	Rr-	Rw	Dr-	Dw	Lr-	Lw	Ur-	Uw				pin 5		pin 3		pin 1	

the blank bits and simply read the *inverse* of the last value written to that bit position in **io** . Read bit **Rr-** means **right** port read handshake when 0; **Rw** means **right** port write when 1. The adjacent bit pairs apply to the **down** , **left** , and **up** ports. Side nodes lack **left** , while top and bottom row nodes lack **up** comm ports. The writable bits of **io** are initialized, on reset, as though the value shown in the "reset" line had been written into the register. The values shown in "WRITE" pertain to general purpose digital I/O pins, if any; the values in "Alt write" are defined by specific peripherals.

GENERAL PURPOSE DIGITAL I/O (GPIO) PINS: If a node has such pins, they are identified by the bit position in **io** at which their state is read. Normal configuration procedures assign pin 17 first, followed by pins 1, 3, and 5 if a node has more than one pin of this type. State is set by writing a value into the two control bits for a pin. All pins reset to weak pulldown. The input bit reads the actual present voltage on the pin, 1 if high, regardless of the selected pin state; the computer is fast enough to directly observe the effects of RLC load circuits.

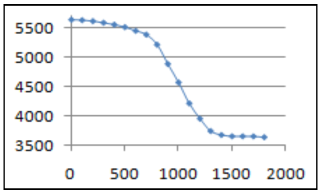
00	High impedance (tristate)
01	Weak pulldown ≈47 KΩ
10	Lo: Sink ≤40mA to Vss
11	Hi: Source ≤40mA from Vdd

PIN WAKEUP: When a side node reads its **left** port address, or a top/bottom node its **up** , the read is suspended while the pin state is not high. To wake on low, write 1 into bit **WD** of **io** . The data from the read is garbage and should be discarded. The pin may be included in a multiport read operation.

Green Arrays™ F18A

I/O and Peripherals

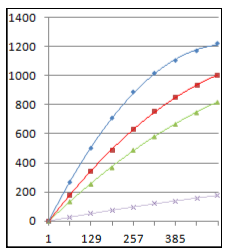
ANALOG INPUT: The F18A analog to digital converter (ADC) is a high speed, free running counter that can be read as **up** or **left** using a special protocol. Its count down frequency varies between ≈3.6GHz for Vdd input and ≈5.6GHz for Vss, as shown in the typical transfer function at right. The **vco ctl** field of **io** selects mode as below, with counter disabled on reset to save power.



00	High impedance input
01	Vdd Calibration
10	Counter disabled
11	Vss Calibration

A voltage is measured in the operating range (≈750mV to ≈1.3v) by calculating the difference between two readings separated by a known time interval. To assist distribution of a time base for sampling and for driving digital signal processing operations, a node with an ADC is supplied with a phantom wakeup pin, always in input mode, used in cooperation with another node.

ANALOG OUTPUT: The digital to analog converter (DAC) is a programmable current source that can be used to generate a voltage across a resistance to ground, or to source an op-amp. By writing the xor of a desired *value* and hex 155 into the low nine bits of **io** that *value* controls the DAC output. A value of 1FF (written as 0AA) sets the DAC for maximum current; a value of 0 (written as 155, the reset state) sets minimum current, high impedance output. The typical DAC transfer functions, in mV versus DAC values, into 75, 50, 37.5 and 8 Ohms are shown at right; as the resistance decreases, the voltage decreases and the function becomes more linear. Analog nodes in F18A based designs have both ADC and DAC connected with separate pins.

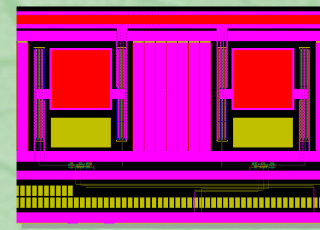


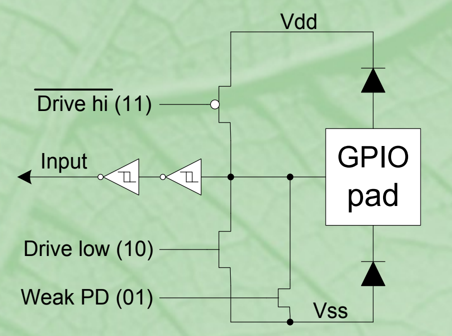
SERDES: The serializer/deserializer peripheral is a high speed (≈450 Mbit/second) transceiver for 18-bit frames using a half duplex two wire medium (clock and data). On reset the SERDES is in input mode. Writing 1 to bit **SR** in **io** sets transmit mode. When in transmit mode, writing a word to **up** is suspended until the previous word has been sent and then begins transmission of the new word. The clock stops if there are no data to transmit. When in receive mode, reading **up** is suspended until data are available. By jumping to **up** a node can execute code received via the SERDES. Additional rules apply for initializing the SERDES and for management of T and S.

18-BIT PARALLEL BUS: This peripheral consists of an 18-bit read/write register addressed as **up** or **left** such that each bit corresponds to an I/O pin. The DB bit in **io** controls bus direction: 1, its reset state, for output; 0 is tristate (high impedance) input. Unlike general purpose pins, reading the port in output mode gives no useful information. A node with this peripheral usually has at least one GPIO pin, or a phantom equivalent, for timing synchronization. In this case, operations on the **up** port wait for pin wakeup while **data** operates immediately regardless of pin state.

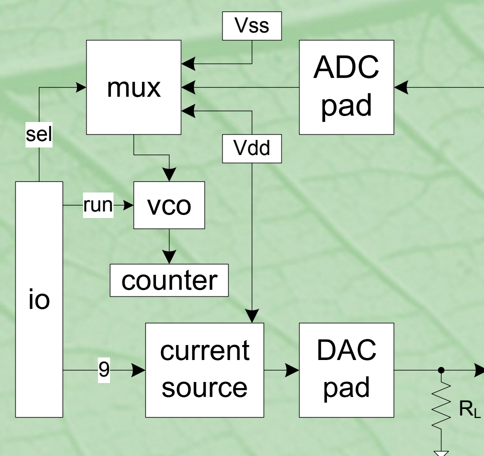
For more information, visit www.GreenArrayChips.com

Two F18A GPIO Pads

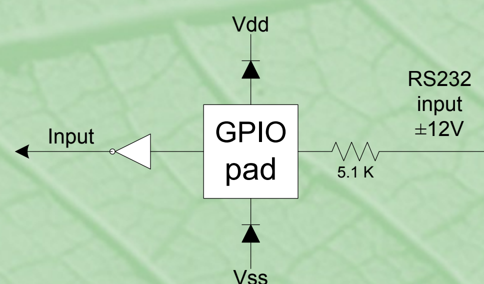




Pin and pad capacitance ≈2.8 pF
Input leakage ≈7 nA (≈250 MΩ)
Short circuit source ≈41 mA, sink ≈41 mA
Weak Pulldown ≈38 µA in saturation



Analog I/O Peripherals



Protection diodes are useful in an RS232 signal receiver

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