Address Space  000-03f RAM (64 words)  040-07f ROM (64 words)  080-0ff I/O ports and registers

<table>
<thead>
<tr>
<th>Port</th>
<th>Address</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-d-u</td>
<td>0fd</td>
<td>Down, Up</td>
</tr>
<tr>
<td>-d--</td>
<td>0f5</td>
<td>Down</td>
</tr>
<tr>
<td>-d IU</td>
<td>0ed</td>
<td>Down, Left, Up</td>
</tr>
<tr>
<td>-d1-</td>
<td>0e5</td>
<td>Down, Left</td>
</tr>
<tr>
<td>---u</td>
<td>0dd</td>
<td>Up</td>
</tr>
<tr>
<td>lo</td>
<td>0d1</td>
<td>I/O Control/Status Register</td>
</tr>
<tr>
<td>--lu</td>
<td>0cd</td>
<td>Left, Up</td>
</tr>
<tr>
<td>--1-</td>
<td>0c5</td>
<td>Left</td>
</tr>
</tbody>
</table>

p 10-bit program register, 6-bit auto-increment
a 18-bit general, address, 6-bit auto-increment
b 8-bit address (write only)

Port Address Description
-0 00b Right, Down, Up
-0s 00s Right, Down
-1 0a1 Right, Down, Left, Up
-1a 0a5 Right, Down, Left
-r-u 09d Right, Up
-r 1 08s Right, Left, Up
-r-l 08s Right, Left

r 18-bit 1+8 return stack
t 18-bit 2+8 data stack
io 18-bit I/O Control and Status Register

Opcode Hex Notes -- ADDRESS opcodes
। 06 return
* 01 execute via r (swap p and r)
name 02 jump to a red word, name
name 03 call to a red word, name
unext 04 jump r=0 decrement r
next 05 jump r=0 decrement r
-if 07 jump t=0

@ 08 literal 6-bit auto-increment
@p 0c fetch via a 6-bit auto-increment
!+ 0d store via a 6-bit auto-increment
!b 0e store via b
! 0f store via a

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<tr>
<td>rd-u</td>
<td>0bd</td>
<td>Right, Down, Up</td>
</tr>
<tr>
<td>rd--</td>
<td>0bs</td>
<td>Right, Down</td>
</tr>
<tr>
<td>rd i</td>
<td>0ad</td>
<td>Right, Down, Left, Up</td>
</tr>
<tr>
<td>rd l</td>
<td>0a5</td>
<td>Right, Down, Left</td>
</tr>
<tr>
<td>r-u</td>
<td>09d</td>
<td>Right, Up</td>
</tr>
<tr>
<td>r</td>
<td>08s</td>
<td>Right, Left, Up</td>
</tr>
<tr>
<td>r-l</td>
<td>08s</td>
<td>Right, Left</td>
</tr>
</tbody>
</table>

Port Address Description
rd-u 0bd Right, Down, Up
rd-- 0bs Right, Down
rd l 0a5 Right, Down, Left
r 09d Right
r-l 08s Right, Left

Opcode Hex Notes -- ALU opcodes
। 10 return
* 11 left shift
2/ 12 right shift (signed)
-o 13 invert (ffff xor)
+ 14 .+ (or add with carry)
and 15 exclusive or (xor)
or 16 .+ (or add with carry)
dup 18

!! 10 .!!
2/ 12 right shift (signed)
+ 14 .+ (or add with carry)

pop 19
over 1a
a 1b fetch from register a

push 1d
b! 1e store into register b
a! 1f store into register a